REMARKS

The Office action mailed on 27 March 2003 (Paper No. 24) has been carefully considered.

Claims 9, 10 and 35 thru 43 are being canceled without prejudice or disclaimer, and claims 1, 2, 4, 5, 11, 17, 18, 23, 24 and 28 are being amended. Thus, claims 1, 2, 4, 5 and 11 thru 34 are pending in the application.

In paragraph 3 of the Office action, the Examiner rejected claims 1, 2, 4, 9 thru 22 and 24 thru 43 under 35 U.S.C. §103 for alleged unpatentability over Berry, U.S. Patent No. 5,150,109 in view of Shiki, U.S. Patent No. 6,292,162. In paragraph 4 of the Office action, the Examiner rejected claims 5 and 23 are rejected under 35 U.S.C. §103 for alleged unpatentability over Berry '109 in view of Shiki '162, and further in view of Kurikko, U.S. Patent No. 5,786,813. For the reasons stated below, it is submitted that the invention recited in the claims, as now amended, is distinguishable from the prior art cited by the Examiner so as to preclude rejection under 35 U.S.C. §103.

Independent claim 1 is being amended to recite the invention with more particularity. In the Office action, the Examiner alleges that the following correspondence exists between elements of claim 1 and elements disclosed in Figure 2 of Berry '109:

Claimed Elements	Elements in Berry '109
Receiver	Master video processor 50
Synchronizing signal generator	Oscillator 52
DAC	Video output DAC 58
Output terminal	Output terminal of DAC 58

There are several distinctions between the invention recited in claim 1 and the disclosure of Berry '109. First, the synchronizing signal generator is recited in claim 1 as having an input connected to an output of the receiver, whereas the oscillator 52 of Figure 2 of Berry '109 has no input, but merely has an output connected to the master video processor 50. Thus, it cannot be said that the oscillator 52 of Berry '109 generates a synchronizing signal "by extracting the synchronizing data from said reconstructed display information" (as recited in claim 1) since the oscillator 52 has no input and receives no input.

Furthermore, claim 1 recites that the output terminal is connected to the synchronizing signal generator as well as to the DAC for transferring the synchronizing signal and the corresponding analog video signal to an analog display apparatus. In contrast, in Berry '109, the output terminal of video output DAC 58 is not connected to the oscillator 52, and thus DAC 58 cannot transfer a synchronizing signal from a synchronizing signal generator to an analog display apparatus.

For the latter reasons, the invention recited in claim 1 is distinguishable from the disclosure of Berry '109, as well as the other references, so as to preclude rejection under 35

U.S.C. §103.

The dependent claims, dependent from claim 1, provide further bases for distinguishing the invention from the prior art cited by the Examiner. For example, referring to dependent claim 4, Berry '109 does not disclose a video data converter (elements 70, 72, 74, 80 and 84, according to the Examiner) connected between the output of a receiver (master video processor 50) and an input of a DAC (video output DAC 58). In fact, the video data converter (70, 72, 74, 80 and 84) of Figure 2 of Berry '109 is not connected at all to the video output DAC 58 thereof.

Referring to claim 5, as amended, that claim recites the analog display apparatus as comprising an amplifier, a deflection signal generator, a high voltage generator, and a cathode ray tube (CRT) display, with the high voltage generator being recited as having an input connected to the deflection signal generator for receiving an output therefrom and for generating a high voltage. In contrast, in Kurikko '813 (Figure 4), cited by the Examiner, the high voltage generator 65 has an input connected to a synchronizing and control unit 60 only, but it does not have an input connected to a deflection signal generator, the latter corresponding (according to the Examiner) to the H-deflection control 63 and the V-deflection control 64. That is to say, the high voltage generator 65 is not at all connected to the deflection control elements 63 and 64 cited by the Examiner.

Referring to dependent claim 11, that claim recites a video data converter connected

between the output of the receiver and an input of the DAC for converting the video data so as to correspond to a prescribed display mode. However, Berry '109 does not disclose a video data converter (70, 72, 74, 80 and 84) connected between an output of a receiver (processor 50) and an input of a DAC (DAC 58).

Turning to consideration of independent claim 2, that claim is also being amended to recite the invention with more particularity. There are several distinctions between the invention recited in claim 2 and the prior art cited by the Examiner.

For example, claim 2 recites a synchronizing signal generator as being connected to an output of the receiver. In contrast, the oscillator 52 of Figure 2 of Berry '109 is not connected to an output of the processor 50, but rather the oscillator 52 only has an output connected to an input of the processor 50. Thus, it cannot be said that the oscillator 52 can perform the function of the synchronizing signal generator recited in claim 2, that is, the function of extracting synchronizing data from reconstructed display information in the processor 50.

Claim 2 also recites the DAC as being connected to an output of the video data converter. In contrast, in Berry '109, the DAC 58 is not at all connected to the output of the video data converter (elements 70, 72, 74, 80 and 84, according to the Examiner). Thus, the DAC 58 of Berry '109 does not perform the function recited in claim 2, that is, the function of converting the converted video data from the video data converter to a corresponding analog video signal.

Finally, claim 2 also recites the output terminal as being connected to an output of the synchronizing signal generator. In contrast, in Berry '109, the output terminal (DAC 58, according to the Examiner) is not at all connected to the output of a synchronizing signal generator (the oscillator 52, according to the Examiner). In fact, the oscillator 52 of Berry '109 has a single output, and that single output is connected to the input of the master video processor 50.

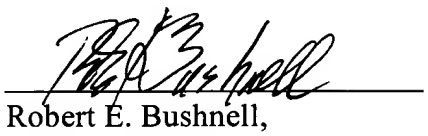
For the latter reasons, it is submitted the invention recited in claim 2 is distinguishable from the prior art cited by the Examiner so as to preclude rejection under 35 U.S.C. §103.

The dependent claims provide further bases for distinguishing the invention from the prior art. For example, in dependent claim 23, the high voltage generator is recited as having an input connected to the deflection signal generator, whereas in Kurikko '813 cited by the Examiner, the high voltage generator 65 (in Figure 4) has an input connected to the synchronizing and control unit 60, but does not have an input connected to the deflection control elements 63 and 64. Thus, this dependent claim provides a further basis for distinguishing the invention from the prior art cited by the Examiner.

In view of the above, it is submitted that the claims of this application are in condition for allowance, and early issuance thereof is solicited. Should any questions remain unresolved, the Examiner is requested to telephone Applicant's attorney.

No fee is incurred by this Amendment.

Respectfully submitted,



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